Electronic Version
Stylesheet Version v1.1.1

Description

METHOD OF IMPROVING ALIGNMENT FOR SEMICONDUCTOR FABRICATION

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates generally to semiconductor processes. More particularly, the present invention relates to a semiconductor process that is capable of improving alignment accuracy and preventing M_0 metal open problem in the alignment mark region.

[0003] 2. Description of the Prior Art

[0004] A DRAM chip is an integrated circuit (IC) made of millions of transistors and capacitors. Typically, a transistor and a capacitor are paired to create a DRAM cell, which represents a single bit of data. The capacitor holds the bit of information -- a "0" or a "1". The transistor acts as a switch that lets the control circuitry on the memory chip read the capacitor or change its state. As known in the art,

memory cells are etched onto a silicon wafer in an array of columns (bitlines) and rows (wordlines). The intersection of a bitline and wordline constitutes the address of the memory cell.

[0005] Briefly, after the formation of the wordlines, a dielectric layer is deposited on the wordlines and in inter-space between these wordlines. Contact holes are etched into the dielectric layer. Metals such as tungsten are deposited inside the contact holes, followed by chemical mechanical polishing (CMP).

[0006] Fig.1 to Fig.4 illustrate the formation of bitline contact devices in the fabrication of a DRAM chip according to the prior art method. As shown in Fig.1, a semiconductor substrate 10 for making a DRAM device is provided having thereon a memory array area 11 and a peripheral area 21. A plurality of wordlines 12, 14, and 16 are defined on the main surface of the semiconductor substrate 10. Alignment mark (AM) 30, which is used to align a photo mask having a contact-hole pattern thereon with the wafer that is mounted on a stepper and scanner, is located in the peripheral area 21 of the semiconductor substrate 10. On the surface of the semiconductor substrate 10, a borophosposilicate glass (BPSG) layer 22 and a TEOS oxide

layer 24 are deposited. A polysilicon layer 26 is deposited on the TEOS oxide layer 24. The polysilicon layer 26 acts as a hard mask in subsequent contact hole etching process.

[0007] As shown in Fig.2, before performing the lithographic process and etching of the bitline contact holes (CB), an alignment window 29 that exposes a portion of the TEOS oxide layer 24 is formed in the polysilicon layer 26. The alignment window 29 is directly located above the alignment mark 30, such that the stepper and scanner may use the alignment mark 30 to align the photo mask with the wafer. To form the alignment window 29, a GV photo resist 28 is formed on the polysilicon layer 26 having an opening located directly above the alignment mark 30. The exposed polysilicon layer 26 is then etched away through the opening. The GC photo resist 28 is removed.

[0008] As shown in Fig.3, after forming the alignment window 29, a CB photo resist 32 is formed on the polysilicon layer 26. Through the alignment window 29 and the alignment mark 30, a mask-wafer alignment is then carried to ensure precise image transfer. Thereafter, by means of exposure and development, a contact hole opening or CB opening 40 is created in the CB photo resist 32.

[0009] As shown in Fig.4, using both the CB photo resist 32 and the polysilicon layer 26 as an etching hard mask, a dry etching process is carried out to etching the bitline contact hole (CB) into the polysilicon layer 26, the TEOS oxide layer 24, and the BPSG layer 22 through the CB opening 40, thereby forming a contact hole 50 between two wordlines 12 and 14. It is noteworthy that this dry etching process simultaneously etches away the TEOS oxide layer 34 and BPSG layer 22 through the alignment window to produce a recess 52 in the peripheral area 21. The subsequent zeroth level (M_0) metallization processes following the formation of contact hole 50 are known in the art. Metal such as tungsten, titanium, or titanium nitride is deposited on the substrate 10 and fills the contact hole 50 and recess 52. Conventional CMP is then carried out to remove metals outside the contact hole 50.

[0010] The above-described prior art process of forming bitline contact hole (CB) has at least two drawbacks. First, although the polysilicon layer 26 that acts as a part of the etching hard mask during the CB etching enables the reduction of the thickness of the CB photoresist and thus improving precision of image transfer, however, the nature of the high diffraction index of the polysilicon layer

26, which might interfere the mask-wafer alignment, is neutralizing this benefit. Secondly, as shown in Fig.5, recess 52 formed in the peripheral area 21 during the etching of the CB contact hole 50 might lead to M_0 metal circuit open after the tungsten CMP process (dishing effect).

SUMMARY OF INVENTION

[0011] Accordingly, it is the primary object of the present invention to provide a semiconductor process to cope with the above-mentioned problems.

[0012] It is another object of the present invention to provide a method for precisely making a bitline contact hole (CB) on a substrate, which is capable of eliminating polysilicon hard mask interference during mask-wafer alignment.

[0013] According to the claimed invention, a semiconductor process capable of improving alignment accuracy is provided. A semiconductor substrate having thereon an array area and a peripheral area is prepared. The array area comprises a plurality of wordlines and the peripheral area comprises at least one alignment mark. At least one dielectric layer is deposited over the array area and the peripheral area. The dielectric layer covers the wordlines and the alignment mark. A thin silicon nitride layer is then deposited on the dielectric layer. A polysilicon layer is de-

posited on the thin silicon nitride layer. A first photo resist layer is coated on the polysilicon layer. An opening is then created in the first photo resist layer by conventional lithographic methods. The opening exposes a portion of the polysilicon layer and is located directly above the alignment mark. A portion of the polysilicon layer is etched away through the opening to form an alignment window in the polysilicon layer. The first photo resist layer is then stripped off. Subsequently, a second photo resist layer is coated on the polysilicon layer. The second photo resist layer fills the alignment window in the polysilicon layer. A contact hole opening is created in the second photo resist layer in said array area by conventional lithographic methods. Using the second photo resist layer, polysilicon layer, and the thin silicon nitride layer as an etching hard mask, a contact hole dry etching process is carried out to etch away the polysilicon layer, thin silicon nitride layer, and the dielectric layer through the contact hole opening in the second photo resist layer, thereby forming a contact hole in the array area.

[0014] It is advantageous that the dielectric layer directly above the alignment mark in the peripheral area is protected by the thin silicon nitride layer during the contact hole dry

etching process.

[0015] Other objects, advantages and novel features of the invention will become more clearly and readily apparent from the following detailed description when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0016] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings:

[0017] Fig.1 to Fig.4 are schematic cross-sectional diagrams illustrating the formation of bitline contact hole (CB) in the fabrication of a DRAM chip according to the prior art method;

[0018] Fig.5 schematically demonstrates the M_0 metal open problem that occurs in the peripheral area directly above the alignment mark (AM) after tungsten CMP according to the prior art; and

[0019] Fig.6 to Fig.9 are schematic cross-sectional diagrams illustrating the formation of a contact plug device during the fabrication of a DRAM chip according to the present

invention.

DETAILED DESCRIPTION

[0020] Please refer to Fig.6 to Fig.9. Fig.6 to Fig.9 are schematic cross-sectional diagrams illustrating the formation of a contact plug device during the fabrication of a DRAM chip according to the preferred embodiment of the present invention, wherein like numerals designate the same or similar regions, layers or elements.

[0021] As shown in Fig.6, a semiconductor substrate 10 is prepared for making a DRAM chip. The semiconductor substrate 10 has at least one array area 11 and one peripheral area 21. A number of wordlines 12, 14, and 16 have been fabricated in the array area 11 on the semiconductor substrate 10. An alignment mark (AM) 30 is defined in the peripheral area 21 of the semiconductor substrate 10. As mentioned, the alignment mark 30 is used to align a photo mask for defining a contact-hole pattern with the semiconductor substrate 10 that is mounted on a wafer stage of lithographic apparatus such as a stepper and scanner. The alignment mark 30 may be specific structure and pattern formed into the semiconductor substrate 10 within the peripheral area 21. On the surface of the semiconductor substrate 10, a borophosposilicate glass (BPSG)

layer 22 and a TEOS oxide layer 24 are deposited.

[0022] A thin silicon nitride layer 25 is then deposited on the TEOS oxide layer 24. A polysilicon layer 26 is deposited on the silicon nitride layer 25. The thin silicon nitride layer 25 and the polysilicon layer 26 constitute a combined hard mask in subsequent contact hole etching process. It is noteworthy that the combined hard mask composed of the thin silicon nitride layer 25 and the polysilicon layer 26 has a lower effective diffraction index than a single polysilicon layer as the prior art. According to the preferred embodiment, the thin silicon nitride layer 25 has a thickness of about 100 angstroms to 300 angstroms.

[0023] As shown in Fig.7, before performing the lithographic process and etching of the bitline contact holes (CB), likewise, an alignment window 29, which exposes a portion of the thin silicon nitride layer 25 and is located directly above the alignment mark 30, is formed in the polysilicon layer 26. The alignment window 29 is directly located above the alignment mark 30 such that the stepper and scanner may use the alignment mark 30 to align the photo mask with the wafer. To form the alignment window 29, a GV photo resist 28 is formed on the polysilicon layer 26 having an opening located directly above the alignment

mark 30. The exposed polysilicon layer 26 is then etched away through the opening. The GC photo resist 28 is removed. The presence of the thin silicon nitride layer 25 laid underneath the polysilicon layer 26 can reduce the interference effect of the polysilicon layer 26 during the mask-wafer alignment.

[0024] As shown in Fig.8, after forming the alignment window 29, a CB photo resist 32 is coated on the polysilicon layer 26. Through the alignment window 29 and the alignment mark 30, a mask-wafer alignment is then carried to ensure precise and accurate image transfer. Thereafter, by means of exposure and development, a contact hole opening or CB opening 40 is created in the CB photo resist 32.

[0025] As shown in Fig.9, using the CB photo resist 32, the polysilicon layer 26 and the thin silicon nitride layer 25 as an etching hard mask, a dry etching process is carried out to etching the bitline contact hole (CB) into the polysilicon layer 26, the thin silicon nitride layer 25, the TEOS oxide layer 24, and the BPSG layer 22 through the CB opening 40, thereby forming a contact hole 50 between two wordlines 12 and 14. Since the thin silicon nitride layer 25 stops the dry etching through the alignment window 29,

there will be no recess defect formed in the peripheral area 21 above the alignment mark 30. The subsequent zeroth level (M_0) metallization processes following the formation of contact hole 50 are then carried out. Metal such as tungsten, titanium, or titanium nitride is deposited on the substrate 10 and fills the contact hole 50 and recess 52. Conventional CMP is then carried out to remove metals outside the contact hole 50.

[0026] Those skilled in the art will readily observe that numerous modification and alterations of the present invention method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.